CLAIMS

1. A nonvolatile semiconductor memory device including a nonvolatile cell circuit comprising:

a step-up circuit for receiving a clock signal to generate a step-up voltage for said nonvolatile cell circuit;

a voltage divider, connected to said step-up circuit, for dividing said step-up voltage to generate a plurality of voltages;

a selector, connected to said voltage divider, for selecting one of said voltages;

a reference voltage generating circuit for generating a reference voltage;

a first comparator, connected to said selector and said reference voltage generating circuit, for comparing said selected one of said voltages with said reference voltage;

a gate circuit, connected to said first comparator and said step-up circuit, for supplying said clock signal to said step-up circuit in accordance with an output signal of said first comparator so that said selected one of said voltages is brought close to said reference voltage;

a second comparator, connected to said step-up circuit, for comparing said step-up voltage with an externally-provided expected value;

a counting signal generating circuit, connected to said second comparator, for generating a counting signal in accordance with an output signal of said first comparator; and

a counter, connected between said counting signal generating circuit and said selector, for changing a value thereof by receiving said counting signal,

said selector selecting said one of said voltages in accordance with said value of said counter, so that said step-up voltage is brought close to said expected value.

2. The nonvolatile semiconductor memory device as set forth in claim 1, wherein said voltage divider comprises a ladder of resistors.

3. The nonvolatile semiconductor memory device as set forth in claim 1, wherein said counter comprises an up counter, said counting signal being a count-up signal.

4. The nonvolatile semiconductor memory device as set forth in claim 1, wherein said counter comprises a down counter, said counting signal being a count-down signal.

5. The nonvolatile semiconductor memory device as set forth in claim 1, wherein said counting signal generating circuit comprises:

a sampling signal generating circuit for generating a sampling signal having a predetermined time period; and

another gate circuit, connected to said sampling signal generating circuit and said second comparator, for passing said sampling signal in accordance with the output signal of said second comparator.

6. The nonvolatile semiconductor memory device as set forth in claim 5, wherein said sampling signal generating circuit comprises:

another counter for receiving said clock signal to generate said sampling signal; and

a further gate circuit, connected to said other counter, for passing said sampling signal in accordance with an externally-provided enable signal.

7. The nonvolatile semiconductor memory device as set forth in claim 6, further comprising a grounded resistor connected to a terminal to which said externally-provided

enable signal is applied.

8. The nonvolatile semiconductor memory device as set forth in claim 1, wherein said nonvolatile cell circuit comprises an adjustment area for storing the value of said counter,

the value of said counter being stored in the adjustment area of said nonvolatile cell circuit after adjustment of the value of said counter is completed,

the value in the adjustment area of said nonvolatile cell circuit being set in said counter in a post-adjustment mode.

9. The nonvolatile semiconductor memory device as set forth in claim 1, further comprising a grounded resistor connected to a terminal to which said externally-provided expected value is applied.